MADE EASY PUBLICATIONS

POSTAL BOOK PACKAGE 2025

CONTENTS

ELECTRONICS ENGINEERING

Objective Practice Sets

Computer Organization

1 CHAPTER
Machine Instructions and Addressing Modes

MCQ and NAT Questions

Q.1 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.2 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?
(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.3 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.
(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.4 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.5 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:
X. Indirect addressing
Y. Indexed addressing
Z. Base register addressing

Column 2:
1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.6 In which of the following address mode, the content of the program counter is added to the address part of the instruction to get the effective address?
(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Q.7 In a certain processor, a 2 byte Jump instruction is encountered at memory address 3010H, the Jump instruction is in PC relative mode. The instruction is JMP – 7 where – 7 is signed byte. Determine the Branch Target Address
(a) 300B H (b) 3009 H
(c) 3003 H (d) 3007 H

Q.8 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	List-II
A. $A[1] = B[J]$;	1. Indirect addressing
B. while [$*A$++];	2. Indexed addressing
C. int temp = $*x$;	3. Auto-increment

Codes:

	A	B	C
(a)	3	2	1
(b)	1	3	2
(c)	2	3	1
(d)	1	2	3

Multiple Select Questions (MSQs)

Q.57 A certain architecture supports indirect, direct and register addressing modes for use in identifying operands for arithmetic instructions. Which of the following can be achieved with a single instruction?

(a) Specifying a register number in the instruction such that the register contains the value of an operand that will be used by the operation.
(b) Specifying a register number in the instruction such that the register will serve as the destination for the operands output.
(c) Specifying an operand value in the instruction such that the value will be used by the operation.
(d) Specifying a memory location in the instruction such that the memory location contains the value of an operand that will be used by the operation.

Q.58 A machine has 24 bit instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. Which of the following are correct?

(a) Total 5 bits are needed for opcode.
(b) The minimum value of immediate operand is –256 if operand is signed integer.
(c) The minimum value of immediate operand is –128 if operand is signed integer.
(d) The maximum value of immediate operand is 255 if operand is signed integer.

Q.59 Consider the following statements. Which of the following is correct for the computers that uses memory mapped I/O?

(a) The computer provides special instruction for manipulating I/O port.
(b) I/O ports are placed at address on bus and as accessed just like other memory location.
(c) To perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.
(d) Ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

■■■■

Answers Machine Instructions and Addressing Modes

1.	(a)	**2.**	(c)	**3.**	(a)	**4.**	(a)	**5.**	(a)	**6.**	(c)	**7.**	(a)
8.	(c)	**9.**	(d)	**10.**	(369)	**11.**	(16383)	**12.**	(b)	**13.**	(b)	**14.**	(d)
15.	(c)	**16.**	(3009)	**17.**	(d)	**18.**	(d)	**19.**	(c)	**20.**	(c)	**21.**	(d)
22.	(c)	**23.**	(b)	**24.**	(c)	**25.**	(d)	**26.**	(b)	**27.**	(c)	**28.**	(b)
29.	(c)	**30.**	(c)	**31.**	(c)	**32.**	(369)	**33.**	(a)	**34.**	(c)	**35.**	(b)
36.	(a)	**37.**	(–128)	**38.**	(a)	**39.**	(a)	**40.**	(d)	**41.**	(a)	**42.**	(d)
43.	(16)	**44.**	(b)	**45.**	(c)	**46.**	(a)	**47.**	(92)	**48.**	(2032)	**49.**	(c)
50.	(a)	**51.**	(b)	**52.**	(c)	**53.**	(c)	**54.**	(2048)	**55.**	(d)	**56.**	(a)
57.	(a, b, d)	**58.**	(c)	**59.**	(b)								

Explanations Machine Instructions and Addressing Modes

2. (c)

Memory size = 4 GB = 2^{32} B
Word size = 2 B

So, unique address = $\frac{2^{32}}{2^1} = 2^{31}$

Hence, atleast 31 bits are required.

3. (a)

Each instruction is stored in one word of memory.

Memory is word addressable and 1 word = 24 bits ⇒ 3 bytes.
Total number bits = 24
The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

4. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

6. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

7. (a)

The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

= 3012 H – 7 H = 300 BH

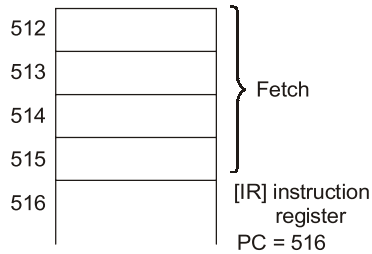
9. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

10. (369)

4 byte instruction storage



Effective address = PC + Relative value

Relative value = EA – PC

= 885 – 516 = (369)10

So, answer is 369.

11. (16383)

(6)	(6)	(6)	
Opcode	R_1	R_2	Immediate

32 – (6 + 6 + 6) = 14 bits for immediate field

$\Rightarrow 2^{14} - 1 = 16383$ maximum possible value of immediate operand.

12. (b)

MDR register needed to read or written data into or onto memory location.

13. (b)

Four address instruction format:

Opcode	A_1	A_2	A_3	A_4
8 bits	24 bits	24 bits	24 bits	24 bits

So total bits needed = (24 bits × 4) + 8 bits

= 96 + 8 bits = 104 bits

So number of bytes = $\frac{104}{8}$ byte = 13 bytes

14. (d)

$M[1000] = 18$, $M[1001] = 1$, $M[1020] = 16$

MOV I R_S, 1	$R_S = 1$
LOAD R_D, 1000 (R_S)	$R_D \leftarrow M[1000+[R_S]]$
	$R_D \leftarrow M[1000+1] = M[1001]$
	$R_D \leftarrow 1$
ADD I R_d, 1000	$R_d \leftarrow R_d + 1000 = 1+1000 = 1001$
STORE I 0(R_d), 20	$M[0+R_d] = 20$
	$M[R_d] = 20$
	$M[1001] = 20$

15. (c)

As the instruction are 24 bit or 3 bytes, the value of program counter at any time should be multiple of 3 starting from 300 like 300, 303, 306 ... from options, '600' is multiple of 3 or is included in above series.

16. (3009)

Word addressable storage

3000 – 3001

3002

3003

3004

3005

3006

3007-3008

3009

Valid program counter value after program is 3009.